



# Search Report

## EIC 2100

STIC Database Tracking Number: 25

**To: CAROLINE ARCOS**  
**Location: RND-5B25**  
**Art Unit: 2195**  
**Thursday, February 14, 2008**

**Case Serial Number: 10/766545**

**From: LUCY PARK**  
**Location: EIC2100**  
**RND-4B28 / RND-4B31**  
**Phone: (571)272-8667**

**lucy.park@uspto.gov**

### Search Notes

Examiner ARCOS:

Here are the results of your Fast & Focused search.

For assistance in retrieving the full text of any patent or article, please send an email to STIC-EIC2100 or call the EIC at 2-4225.

Please don't hesitate to contact me if you have any questions about the search.

Thank you,  
Lucy

Lucy Park  
NPL/Patent Searcher  
EIC 2100



EIC 2100 251357  
**FAST & FOCUSED SEARCH**

Today's Date 2/14/08

**This search cannot be completed unless you:**

**A. Attach a copy of your EAST strategy.**

**B. Conduct an interview with your searcher.**

Name Caroline Acres

Priority App. Filing Date 1/27/2004

AUI/Org. 2195 Examiner # 83774

Case/App. # 10/766-545

Bld.&Rm.# 5825 Phone 571-270-3151

**Format for Search Results**

EMAIL \_\_\_\_\_ PAPER X

If this is a Board of Appeals case, check here ☐

Synonyms \_\_\_\_\_

Describe this invention in your own words part of a thread (module) to cause another to be loop and consider both module as 1 thread  
1st module invokes (TMCs) to point to 1st instruction of 2nd module  
2nd module register 1st events of interest with (event Ns)

Terms to avoid \_\_\_\_\_

Additional Comments

Please hand deliver completed form to your TIS.

**STIC USE ONLY**

Searcher WeyPark

Date Completed 2-14-08

Phone 28667

Sources Galaxy

# STIC Search Results Feedback Form

**EIC 2100**

Questions about the scope or the results of the search? Contact *the EIC searcher or contact:*

Alyson Dill, EIC 2100 Team Leader  
272-3527, RND 4B28

## Voluntary Results Feedback Form

*D I am an examiner in Art Unit::*

Example: 2133

*D Relevant prior art found, search results used as follows:*

- ☐ 102 rejection Publication number cited or NPL citation \_\_\_\_\_
- ☐ 103 rejection Publication number cited or NPL citation \_\_\_\_\_
- ☐ Cited as being of interest. Publication number cited or NPL citation \_\_\_\_\_
- ☐ Helped examiner better understand the invention.
- ☐ Helped examiner better understand the state of the art in their technology.

*Types of relevant prior art found:*

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature  
(Journal articles, conference proceedings, new product announcements etc.)

*D Relevant prior art not found:*

- ☐ Results verified the lack of relevant prior art (helped determine patentability).
- ☐ Results were not useful in determining patentability or understanding the invention.

*Comments:*

**Drop off or send completed forms to STIC/EIC2100 RND, 4B28**

[File 347] **JAPIO** Dec 1976-2007/Oct(Updated 080129)

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*\*File 347: File Histories now available for ordering when searching via DialogLink 5 and Web products, see HELP FILEHIST for more information.*

[File 350] **Derwent WPIX** 1963-2008/UD=200810

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*\*File 350: Chinese Utility Model registrations in English now available To order File Histories, see HELP FILEHIST for details.*

; d s

Set Items Postings Description

S1 3261446 11717965 S THREAD??? OR MULTITHREAD? OR PROCESS OR PROCESSES

S2 42846 313184 S (MODULE? ? OR UNIT? ? OR BLOCK? ? OR SET? ? OR GROUP??? OR

COLLECTION? ?)(3N)INSTRUCTION? ?

S3 3352 41513 S S2(3N)(TWO OR SECOND??? OR 2ND OR PAIR OR COUPLE OR TWIN OR DUAL  
OR ANOTHER OR SEPARATE)

S4 169 1957 S S3(3N)(CHAIN??? OR BIND??? OR BOUND? OR LOOP??? OR CONNECT??? OR  
ATTACH???? OR TIE? ?)

S5 4228 35772 S (EVENT? ? OR ACTION? ? OR OCCURRENCE? ?)(3N)(NOTIFY??? OR NOTIFIE? ?  
OR NOTIFICATION? ? OR ALERT???)

S6 0 0 S SI AND S4 AND S5

S7 67 1265 S S1 AND S4

S8 5 165 S S7 AND THREAD???

S9 0 0 S S4 AND S5

S10 0 0 S SI AND S3 AND S5

S11 1095 17874 S S1 AND S5

S12 36 815 S S1 I AND S2

S13 36 815 S S12 NOT S8

S14 17 426 S S13 NOT AD=20040126:20080214/PR

S15 2963 37409 S S2(3N)(TWO OR SECOND??? OR 2ND OR SEPARATE)

S16 152 1772 S S15(3N)(CHAIN??? OR BIND??? OR BOUND? OR LOOP??? OR CONNECT??? OR  
ATTACH???? OR TIE? ?)

S17 54 1012 S S16 AND S1

S18 51 959 S S17 NOT AD=20040126:20080214/PR

S19 50 944 S S18 NOT (S8 OR S14)

8/3,K/2 (Item 2 from file: 350) Links

Fulltext available through: [Order File History](#)

Derwent WPIX

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0010999896 & & *Drawing available*

WPI Acc no: 2001-625035/200172

XRPX Acc No: N2001-465795

Automatic distributed **processing system in computer network**, appends new instruction generated by server **upon processing current instruction from client, with thread identifier**

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: MURAMATSU K

Patent Family 2 patents, 2 & countries

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20010027462	A1	20011004	US 2001817259	A	20010327	200172	B
JP 2001273156	A	20011005	JP 200088703	A	20000328	200173	E

Priority Applications (no., kind, date): JP 200088703 A 20000328

Patent Details

Patent Number	Kind	Lang	Pgs	Draw	Filing Notes
US 20010027462	A1	EN	18	11	
JP 2001273156	A	JA	11		

...computer network, appends new **instruction** generated by **server upon** processing current **instruction from client, with thread identifier** Alerting Abstract ...NOVELTY - Server (21) that generates an instruction during processing of an application, appends a **thread** identifier to the instruction and sends it to client (31). Client creates a thread to process the received instruction in collaboration with a higher-level library of client. New instruction generated upon processing the received instruction, is appended with the **thread** identifier and sent to server. ...ADVANTAGE - Deadlock caused by distributed **processes** is avoided by appending new instruction, which is generated by the server during processing of current instruction on the client, with the **thread** identifier of the current instruction and sending to the server... **Title Terms** .../Index Terms/Additional Words: **PROCESS**; ...**...THREAD**; Original Publication Data by Authority...Original Abstracts:to a client via a network has a relay library which includes an instruction relay thread which appends a **thread** identifier to an instruction, which is generated during processing of an application, and relays the instruction in collaboration with a higher-level library, and an instruction distribution thread for searching for a **thread** that processes another **instruction** from the client. The client has an instruction execution module including an instruction distribution **thread** for receiving the instruction with the **thread** identifier, creating a **thread** that processes the **instruction**, and passing the instruction to that thread with the **thread identifier**, and an instruction processing **thread** for processing the received instruction in collaboration with a higher-level library, and for, when another instruction is generated during the instruction process or the instruction process is complete, sending the other instruction appended with the **thread** identifier to the **instruction** distribution thread. ...Claims:automatic distributed processing system comprising: a server machine including: an instruction relay library comprising: a thread management table for storing thread identifiers in correspondence with **threads**; a server instruction relay **thread** for, when an instruction is generated during processing of an application, appending a **thread** identifier managed by said thread management table to the instruction, and sending the instruction to a client machine in collaboration with a higher-level library of said server machine; and a server instruction distribution **thread** for distributing a **thread** which **processes** another instruction from the client machine; and a client machine connected to said server machine via a network, said **client** machine including: an **instruction** execution module comprising: a client **instruction** distribution **thread** for receiving the instruction sent from said instruction relay thread of said server machine together with the thread identifier, creating a thread that processes the instruction, and passing the received instruction to the created thread together

with the **thread** identifier; and an **instruction** processing **thread** for **processing** the **received** instruction in collaboration with a higher-level library of said **client** machine, and for, **when** another instruction is generated upon processing the **received** instruction or the processing of the received instruction is complete, sending the other instruction or a processing end reply appended with the **thread** identifier to said instruction distribution **thread** of said server machine.

8/3,K/4 (Item 4 from file: 350) [Links](#)

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Derwent WPIX

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0007759298 & & *Drawing available*

WPI Acc no: 1996-384091/199638

**Multistream instruction processor able to reduce** interlocks - has instruction stream controller with event detector, context backup **memory and exchange controller for extracting first instruction from thread and** replacing it with **second instruction stream**

Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)

Inventor: HIRATA H; KIMURA K

Patent Family 1 patents, 1 & countries

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5546593	A	19960813	US 199363938	A	19930517	199638	B

Priority Applications (no., kind, date): JP 1992124910 A 19920518

Patent Details

Patent Number	Kind	Lang	Pgs	Draw	Filing Notes
US 5546593	A	EN	24	11	

...**controller with event** detector, context backup memory and exchange **controller for** extracting first instruction from thread and replacing it with second instruction stream Alerting Abstract ...thread slots which fetch and decode instructions from an assigned ...decoding result of the **threaded** slot. An execution connection... ..placed into the thread slot which was used by the first... ..USE/ADVANTAGE - effectively than the multithread processor by suppressing **Title Terms** .../Index Terms/Additional Words: **THREAD**; Original Publication Data by Authority...Original Abstracts:instruction streams is N or larger than N. Such processor comprises aninstructionpreparationunit comprised of N **thread** slots each of which fetches/decodes instructions from the instruction stream assigned thereto as well as issues decoding result... .. execution units each of which executes instructions in accordance with the decoding result of the **thread** slot; an execution connection unit for replacing a connection with another, the connection between **the instruction preparation unit and the functional unit** so that the result received from the **thread** slot will be provided to the execution unit which is ready to execute it; and an instruction stream controller... ..Claims:is N and larger than N, the processor comprising:an instruction preparation unit comprised of thread slots each of which fetches and decodes instructions from the instruction stream assigned thereto as well as issues a decoding result one at a time, the number of the thread slots being N;a functional unit comprised of instruction execution means each of which executes the instructions in accordance with the decoding result of the **thread** slot, the number of the instruction execution means being M, the functional unit including at least one delayable execution means;an execution connection unit... .. instruction preparation unit and the functional unit so that the decoding result received from the thread slot will be provided to the instruction execution means which is ready to execute it; andan instruction stream controller comprised of an event detector... .. of the instruction stream had been conducted prior to the execution delay, the context including thread slot context information indicating an operation state of the thread slot assigned to the instruction stream and execution means context information indicating an operation state of the delayable execution means so that the instruction stream may later be returned to a **thread** slot and the delaying instruction may be immediately re-executed in the delayable execution means; andthe exchange controller performing the following functions when the event detector detects... .. stream,extracting the context of the first instruction stream, including the first instruction stream's thread slot context information and execution means context information, and temporarily storing it into the context backup memory,putting a second instruction stream into the thread slot that was assigned to the first instruction stream by using the second instruction stream's thread slot context information, andmaking the delayable execution means directly receive and immediately execute the **second** instruction stream's delaying

14/5/8 (Item 8 from file: 350) [Links](#)

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Derwent WPIX

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0009501193 & *Drawing available*

WPI Acc no: 1999-443742/199937

XRPX Acc No: N1999-330962

Customized software updating **method in generic** software application

Patent Assignee: ORACLE CORP (ORAC-N)

Inventor: WALLACK P

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5933645	A	19990803	US 1996618126	A	19960319	199937	B

Priority Applications (no., kind, date): US 1996618126 A 19960319

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5933645	A	EN	16	9	

Alerting Abstract US A

NOVELTY - An updated version of a software application is executed by receiving an **event notification** message and selecting an independent custom event handler or a default event handler, based on a co-ordination style. An automatic integration of the updated version with computer readable instructions of the independent custom handler is performed during the execution **process**.

DESCRIPTION - The updated version includes a group of executable instruction. The software application generates the event notification message for a predefined significant event in the software application and the default event handler for execution in response to the predefined significant event. A state of variables and parameters for the software application are recorded before and after execution of the custom event handler. A difference between the state of variables and parameters is determined after execution of the custom event handler, recorded in a debug file and displayed on a display screen. INDEPENDENT CLAIMS are also included for the following:

A. customized software upgrading system;

B. computer readable medium

USE - For upgrading customized software, for non-invasive extensions in generic software applications.

ADVANTAGE - As the software applications are customized by selecting either independent custom handler or default handler based on received co-ordinate style, the modification of application source code is not necessary, thereby software support is facilitated by isolating vendor supplied application program from user customization, eliminating complicative processes and increasing the overall efficiency of the **system**.

DESCRIPTION OF DRAWINGS - The figure shows a computer system that accommodates non-invasive extensions to software application.



19/5/7 (Item 7 from file: 350) [Links](#)

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Derwent WPIX

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0013101464 & *Drawing available*

WPI Acc no: 2003-182745/200318

XRPX Acc No: N2003-143776

**Primary instruction set processing method involves executing** secondary instruction set in response to counter invoked by branch instruction **of primary instruction set**

Patent Assignee: ALTMAN E R (ALTM-I); GLOSSNER C J (GLOS-I); HOKENEK E (HOKE-I); IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC); MELTZER D (MELT-I); MOUDGILL M (MOUD-I)

Inventor: ALTMAN E R; GLOSSNER C J; HOKENEK E; MELTZER D; MOUDGILL M; DAVID M; ERDEM H; MAYAN M

Patent Family ( 5 patents, 23 & countries )

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20020161987	A1	20021031	US 2001845693	A	20010430	200318	B
WO 2002088941	A1	20021107	WO 2002US13394	A	20020426	200318	E
EP 1384146	AI	20040128	EP 2002729032	A	20020426	200409	E
			WO 2002US13394	A	20020426		
CN 1505781	A	20040616	CN 2002808973	A	20020426	200465	
CN 1243305	C	20060222	CN 2002808973	A	20020426	200664	

Priority Applications (no., kind, date): US 2001845693 A 20010430

Patent Details

Patent Number	Kind	Lang	Pgs	Draw	Filing Notes	
US 20020161987	AI	EN	10	4		
WO 2002088941	AI	EN				
National Designated States,Original	CA CN DE GB					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR					
EP 1384146	AI	EN			PCT Application	WO 2002US13394
					Based on OPI patent	WO 2002088941
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR					

Alerting Abstract US AI

NOVELTY - A secondary instruction set is stored in buffers connected to respective execution units (301-305). The secondary instruction set is executed in response to a counter invoked by a branch instruction of a primary instruction set.

DESCRIPTION - An INDEPENDENT CLAIM is included for processor.

USE - For processing primary instruction set.

ADVANTAGE - By executing the secondary instruction set in response to branch instruction of primary instruction set, the potential instruction pipeline completion rate is achieved without instruction fetch bandwidth limitation.

DESCRIPTION OF DRAWINGS - The figure shows the processor.

301-305 Execution units

[File 2] **INSPEC** 1898-2008/Jan W2  
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[File 6] **NTIS** 1964-2008/Feb W3  
(c) 2008 NTIS, Intl Cpyrght All Rights Res. All rights reserved.

[File 8] **Ei Compendex(R)** 1884-2008/Jan W4  
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[File 23] **CSA Technology Research Database** 1963-2008/Jan  
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[File 34] **SciSearch(R) Cited Ref Sci** 1990-2008/Feb W3  
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[File 35] Dissertation **Abs Online** 1861-2007/Oct  
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[File 65] Inside **Conferences** 1993-2008/Feb 12  
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[File 95] **TEME-Technology & Management** 1989-2008/Feb W1  
(c) 2008 FIZ TECHNIK. All rights reserved.

[File 99] Wilson Appl. Sci & Tech Abs 1983-2008/Jan  
(c) 2008 The HW Wilson Co. All rights reserved.

[File 144] Pascal 1973-2008/Feb W1  
(c) 2008 INIST/CNRS. All rights reserved.

[File 434] **SciSearch(R) Cited Ref Sci** 1974-1989/Dec  
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W5tY<sup>Y</sup>c3r1

; d s

Set Items Postings Description

S1 7842864 13595375 S THREAD??? OR MULTITHREAD? OR PROCESS OR PROCESSES  
S2 34655 110434 S (MODULE? ? OR UNIT? ? OR BLOCK? ? OR SET? ? OR GROUP??? OR  
COLLECTION? ?)(3N)INSTRUCTION? ?  
S3 1197 4195 S S2(3N)(TWO OR SECOND??? OR 2ND OR PAIR OR COUPLE OR TWIN OR DUAL  
OR ANOTHER OR SEPARATE)  
S4 0 0 S S3(3N)(CHAIN??? OR BIND??? OR BOUND? OR LOOP??? OR CONNECT??? OR  
ATTACH??? OR TIE? ?)  
S5 2127 6012 S (EVENT? ? OR ACTION? ? OR OCCURRENCE? ?)(3N)(NOTIFY??? OR NOTIFY? ?  
OR NOTIFICATION? ? OR ALERT???)  
S6 0 0 S SI AND S3 AND S5  
S7 5149 26589 S SI AND S2  
S8 0 0 S S7 AND S5  
S9 4876 13351 S (MODULE? ? OR UNIT? ?)(3N)INSTRUCTION?  
S10 50 152 S S9(5N)(CHAIN??? OR BIND??? OR BOUND? OR LOOP??? OR CONNECT??? OR  
ATTACH??? OR TIE? ?)  
S11 4 22 S SIO AND S1  
S12 4 22 RD (unique items)  
S13 0 0 S SIO AND S5

[File 348] **EUROPEAN PATENTS** 1978-2007 / 200806

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\*File 348: For IPCR/8 information, see **HELP NEWSIPCR**. To order File Histories, see **HELP FILEHIST** for details.

[File 349] **PCT FULLTEXT** 1979-2008/UB=20080131UT=20080124

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\*File 349: For IPCR/8 information, see **HELP NEWSIPCR**. To order File Histories, see **HELP FILEHIST** for details.

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Set Items Postings Description

S1 1506766 19955242 S THREAD??? OR MULTITHREAD? OR PROCESS OR PROCESSES  
S2 49064 602620 S (MODULE? ? OR UNIT? ? OR BLOCK? ? OR SET? ? OR GROUP??? OR  
COLLECTION? ?)(3N)INSTRUCTION? ?  
S3 4155 49523 S S2(3N)(TWO OR SECOND??? OR 2ND OR PAIR OR COUPLE OR TWIN OR DUAL  
OR ANOTHER OR SEPARATE)  
S4 139 1180 S S3(3N)(CHAIN??? OR BIND??? OR BOUND? OR LOOP??? OR CONNECT??? OR  
ATTACH???? OR TIE? ?)  
S5 9442 81918 S (EVENT? ? OR ACTION? ? OR OCCURRENCE? ?)(3N)(NOTIFY??? OR NOTIFIE? ?  
OR NOTIFICATION? ? OR ALERT???)  
S6 0 0 S S1(100N)S4(100N)S5  
S7 5 63 S S1(50N)S4  
S8 2 27 S S1(100N)S3(100N)S5  
S9 0 0 S S8 NOT S7  
S10 157 2297 S S1(100N)S3(15N)(CHAIN??? OR BIND??? OR BOUND? OR LOOP??? OR  
CONNECT??? OR ATTACH???? OR TIE? ?)  
S11 0 0 S S10(100N)S5  
S12 14 436 S S10(100N)EVENT?  
S13 11 105 S S12 NOT S7  
S14 8 70 S S13 NOT AD=20040126:20080214/PR  
S15 21874 234926 S (MODULE? ? OR UNIT? ?)(3N)INSTRUCTION? ?  
S16 861 7660 S S15(5N)(CHAIN??? OR BIND??? OR BOUND? OR LOOP??? OR CONNECT??? OR  
ATTACH???? OR TIE? ?)  
S17 15 222 S S16(100N)(THREAD??? OR MULTITHREAD???)  
S18 15 222 S S17 NOT (S7 OR S13)  
S19 10 112 S S18 NOT AD=20040126:20080214/P

at-  
patents

1413K/4 (Item 4 from file: 348) [Links](#)

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EUROPEAN PATENTS

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00839285

System and method for **simulation of computer systems** combining hardware and software interaction

Anordnung und Verfahren zur Simulation von Rechnersystemen mit kombinierter Hardware- und Software-Interaktion

Système et méthode pour la simulation de systèmes d'ordinateur combinant une interaction entre matériel et logiciel

Patent Assignee:

C. Eagle **Design Automation, Inc.**; (2230010)

12415 S.W. Millikan Way; Beaverton, Oregon 97005; (US)

(applicant designated states: AT;BE;CH;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)

Inventor:

D. **Bunza, Geoffrey J.**

9350 S.W. Pine Street; Beaverton, Oregon 97005; (US)

Legal Representative:

E. **Grunecker, Kinkeldey, Stockmair & Schwanhauser Anwaltssozietat** (100721)

Maximilianstrasse 58; 80538 Munchen; (DE)

	Country	Number	Kind	Date	
Patent	EP	777180	A2	19970604	(Basic)
	EP	777180	A3	19990210	
Application	EP	96119099		19961128	
Priorities	US	566401		19951201	

Designated States:

AT; BE; CH; DE; DK; ES; FI; FR; GB; GR;

IE; IT; LI; LU; MC; NL; PT; SE;

International Patent Class (V7): G06F-011/26; ;

Type	Pub. Date	Kind	Text
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Publication: English

Procedural: English

Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB97	3451
SPEC A	(English)	EPAB97	8800
Total Word Count (Document A) 12251			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 12251			

Claims: ...to control communications between said first processor emulator and said hardware simulator only on said event when the target program for the first target microprocessor requires interaction ...to control communications between said second processor emulator and said hardware simulator only on said event when the target program for the second target microprocessor requires interaction with the target circuitry... ..and second processor emulators are each coupled to said hardware simulator by a computer network connection, said communications interface controlling communications over said network connections.

19. The system of claim 16... ..coupled to said first and second processor emulators, respectively, said first exception detector detecting said event when the target program for the first target microprocessor requires interaction with the target circuitry, and said second exception detector detecting said event when the target program for the second target microprocessor requires interaction with the target circuitry... ..detector temporarily halts execution of said first set of computer instructions while said hardware simulator processes said event when the target program for the first target microprocessor requires interaction with the target circuitry, and said second exception detector temporarily halts execution of said second set of computer instructions while said hardware simulator processes said event when the target program for the second target microprocessor requires interaction with the target circuitry.

21. The system of claim 16 wherein said event when the target program for the first target microprocessor requires interaction with the target circuitry... ..first processor emulator to said hardware simulator.

22. The system of claim 16 wherein said event when the target program for the second target microprocessor requires interaction with the target circuitry...

14/3K/6 (Item 1 from file: 349) [Links](#)

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PCT FULLTEXT

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01073106

**METHOD AND APPARATUS FOR REAL-TIME MULTITHREADING**  
**PROCEDE ET DISPOSITIF DE TRAITEMENT MULTIPLE EN TEMPS REEL**

**Patent Applicant/Patent Assignee:**

**F. UNIVERSITY OF DELAWARE;** Office of the Vice Provost for Research, 210 Hulliher Hall, Newark, DE

19716

US; US(Residence); US(Nationality)

(For all designated states except: US)

**G. GAO Guang R;** 6 Haywood Court, Newark, DE 19711

US; US(Residence); CA(Nationality)

**H. THEOBALD Kevin B;** 1492 Northeast Alex Way, Apartment 316, Hillsboro, OR 97124

US; US(Residence); US(Nationality)

**Patent Applicant/Inventor:**

**I. GAO Guang R**

6 Haywood Court, Newark, DE 19711; US; US(Residence); CA(Nationality);

**J. THEOBALD Kevin B**

1492 Northeast Alex Way, Apartment 316, Hillsboro, OR 97124; US; US(Residence); US(Nationality);

**Legal Representative:**

**K. OLSEN James M(agent)**

Connolly Bove Lodge & Hutz LLP, P.O. Box 2207, Wilmington, DE 19899-2207; US;

	Country	Number	Kind	Date
Patent		2003102758	AI	20031211
Application	WO	2003US17223		20030530
Priorities	US	2002384495		20020531

**Designated States:** (All protection types applied unless otherwise stated - for applications 2004+)

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;

FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;

PT; RO; SE; SI; SK; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;

ML; MR; NE; SN; TD; TG;

IAN GH; GM; KE; LS; MW; MZ; SD; SL; SZ; TZ;

UG; ZM; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English

Filing Language: English

**Detailed Description:**

...wireless communications equipment, personal digital assistants (PDAs), network switches and routers, etc.

By keeping the **multithreading unit separate** from the instruction processor in the present invention, a small amount of extra time is spent in their interaction, compared to a design in which **multithreading** capability is integral to the processor.

This trade-off is acceptable as it leads to... ..the advantage of leveraging off-the-shelf processor design and technology.

Because the model of **multithreading** in the present invention differs from

.4

other models of parallel synchronization, it involves distinct programming... ..described herein, the invention comprises a computer-implemented apparatus comprising: one or more multithreading nodes **connected** by an interconnection network, each multithreading node comprising: an execution unit (EU) for executing active... ..fibers and procedures, and handling remote accesses; two queues, the ready queue (RQ) and the event queue (EQ), through which the EU and SU communicate, the ready queue providing information received... ..synchronization unit to the at least one computer processor of the execution unit, and the **event queue** providing information received -from the at least one computer processor of the execution unit...

19/3K/2 (Item 2 from file: 348) [Links](#)

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EUROPEAN PATENTS

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**METHOD AND APPARATUS FOR SELECTING THREAD SWITCH EVENTS IN A MULTITHREADED PROCESSOR**

VERFAHREN UND GERAET ZUM WAEHLEN VON FADENWECHSELEREIGNISSEN IN EINEM MEHRFADENPROZESSOR

PROCEDE ET APPAREIL DE SELECTION D'EVENEMENTS DE COMMUTATION D'UNITES D'EXECUTION DANS UN PROCESEUR A UNITES D'EXECUTION MULTIPLES

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Specification: ...suspended in response to, for example, the occurrence of L1 D-cache miss, a second **thread** would be able to access the L1 D-cache 120 for data present therein. If the second thread also results in L1 D-cache miss, another data request will be issued and thus....Cache. The storage control unit 200, the execution units 260, 270, and 280 and the instruction **unit** 220 are all operationally **connected** to the thread switch logic 400 which determines which **thread** to execute.

As illustrated in Figure 2, a bus 205 is provided between the storage...